

Appl. No. 09/525,615

Doc. Ref.: AQ57

PATENT ABSTRACTS OF JAPAN(11)Publication number : **05-327356**(43)Date of publication of application : **10.12.1993**

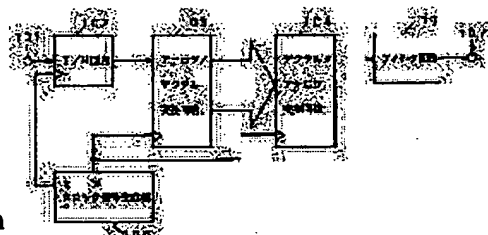
(51)Int.Cl.

H03D 7/00

(21)Application number : **04-130898**(71)Applicant : **SANYO ELECTRIC CO LTD
TOTTORI SANYO ELECTRIC CO
LTD**(22)Date of filing : **22.05.1992**(72)Inventor : **IINUMA TOSHINORI
KOSAKA AKIO****(54) FREQUENCY CONVERTER****(57)Abstract:**

PURPOSE: To miniaturize the device and to reduce energy consumption by sampling an input signal at the cycle of a frequency lower than the double of the lowest frequency of the input Signal, converting the input signal to a digital signal and integrating it into a digital IC.

CONSTITUTION: A signal not containing a low frequency component is inputted to an input terminal 101 and temporarily held at a trace/hold (T/H) circuit 102. A clock signal, whose frequency is lower than the double of the lowest frequency of the input signal, is generated by a clock signal generator 106. This control clock signal (1) is supplied to the T/H circuit 102, and a sampling clock signal (2) a little delayed rather than the control clock signal (1) is supplied to an A/D converter 103 and a D/A converter 104. Thus, the input signal is sampled, and A/D converted outputs are turned to the amplitude data of frequency converted signals. By integrating this device into the digital IC, the device can be miniaturized, and the energy consumption can be reduced.

**LEGAL STATUS**

[Date of request for examination] 07.07.1998

[Date of sending the examiner's decision of rejection] 24.04.2001

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of extinction of right]

Copyright (C); 1998,2003 Japan Patent Office